IN THE DRAWINGS:

The attached drawings include changes to FIGS. 1 and 2a-2c to show designation by a legend of --PRIOR ART---. The sheets containing FIG. 1 and 2a-2c replace the original sheets including FIGs. 1 and 2a-2c. Approval of these changes to the Drawings is respectfully requested.

REMARKS

INTRODUCTION:

In accordance with the foregoing, claims 1, 6, 10 and 11 have been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-15 are pending and under consideration. Reconsideration is respectfully requested.

OBJECTIONS TO THE DRAWINGS:

In the Office Action, at page 2, the drawings were objected to. Corrections to FIGS. 1 and 2a-2c have been requested and replacement figures have been submitted herewith. Therefore, the outstanding drawing objections should be resolved.

Reconsideration and withdrawal of the outstanding objections to the drawings are respectfully requested.

REJECTION UNDER 35 U.S.C. §102:

In the Office Action, at pages 2-5, claims 1-3 and 6-15 were rejected under 35 U.S.C. §102(e) as being anticipated by Kurokawa et al. (USPN 6,621,130; hereafter, Kurokawa). This rejection is traversed and reconsideration is requested.

For clarity, independent claim 1 has been amended to recite, in part: "a floating gate dielectric layer formed between the adjacent field oxide layers, wherein the floating gate dielectric layer includes a first dielectric layer and a second dielectric layer which are connected and positioned in parallel between a source and a drain formed on the substrate, and the thickness of the first dielectric layer is thicker than the second dielectric layer."

It is respectfully submitted that, as described more fully below, a significant difference between the present claimed invention and Kurokawa is a connectional and positional relationship of a first dielectric layer 24a in parallel with a second dielectric layer 24b between a source 22 and drain 23 in the present invention and a connectional and positional relationship of a first dielectric layer 106 in series with a second dielectric layer 207 between a source 103 and a drain 104 in Kurokawa. That is, the first dielectric layer 24a and the second dielectric layer 24b of the present invention are connected and positioned in a parallel relationship with respect to the source 22 and the drain 23, which is illustrated in Figs. A and B on the next page:

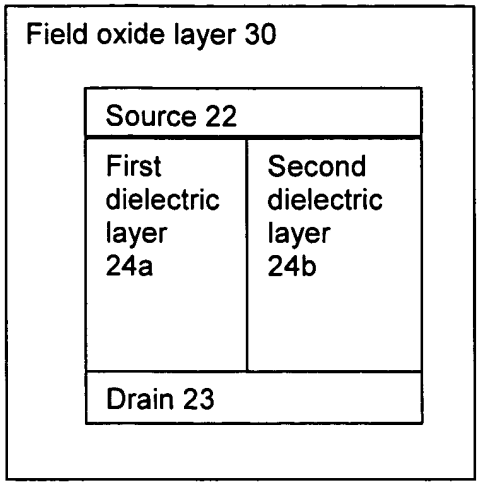

Fig. A

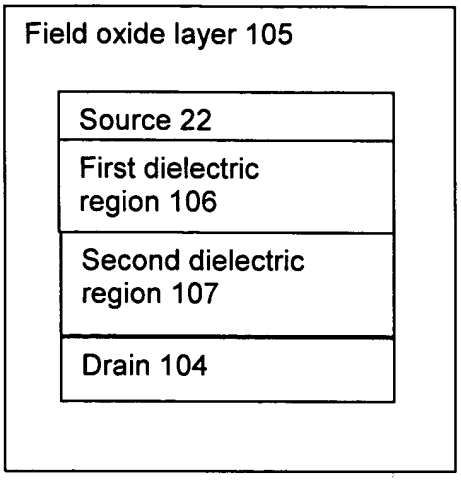

Fig. B

In detail, as shown in Figs. 4b, 4c and claim 1 of the present invention, the flash EEPROM unit cell of the present invention comprises: a substrate 21, on which field oxide layers 30 are formed for isolating unit cells; a floating gate dielectric layer 24a, 24b formed between the adjacent field oxide layers 30; a floating gate 25 formed on the floating gate dielectric layer 26 formed on the floating gate 25; and a control gate 27 formed on the control gate dielectric layer 26.

The floating gate dielectric layer 24a, 24b includes the first dielectric layer 24a and the second dielectric layer 24b, which are positioned and connected in parallel between a source 22 and a drain 23 formed on the substrate 21, and the thickness of the first dielectric layer 24a is thicker than the second dielectric layer 24b. The positional relationships (plane view) of the first dielectric layer 24a, the second dielectric layer 24b, the source 22, the drain 23, and the field oxide layers 30 of the present invention are illustrated in Fig. A.

In contrast, in Figs. 1A-1C and claim 1 of Kurokawa, the flash EEPROM unit cell comprises: an active layer having a drain region 104, a source region 103, and a channel forming region 102 formed over a substrate 101; a first region 106 and a second region 107 formed in the channel forming region 102; a first insulating film (a tunnel oxide film) 108 formed on the active layer; a floating gate 109 formed on the first insulating film 108; a second insulating film 110 formed on the floating gate 109; and a control gate 111 formed on the second insulating film 110.

A concentration of impurity elements in the first region 106 is larger than a concentration of impurity elements in the second region 107, and a thickness of the first insulating film (a tunnel oxide film) 108 on the second region 107 is thinner than a thickness of the second

insulating film (a tunnel oxide film) 108 on the first region 106. The positional relationship (plane view) of the first insulating film (a tunnel oxide film) 108, the second insulating film (a tunnel oxide film) 110, the source 103, the drain 104, and a field oxide layer 105 are illustrated in Fig. B.

An advantage or effect that results from the parallel relationship between the source 22 and the drain 23 in the present invention is that the gate-coupling ratio (GCR) is increased or the cell size is reduced while maintaining the GCR value.

In particular, the GCR is important in determining the operating voltage of the unit cell, and may be expressed by the following equation (see paragraphs [0007}. {0008]):

$$GCR = C1 / (C1 + C2)$$

In the above equation, C1 represents a capacitance between the floating gate 15 and the control gate 17, and C2 represents a capacitance between the floating gate 15 and the substrate 11. Capacitance is proportional to the dielectric constant and the area of a dielectric layer and is inversely proportional to the thickness of the dielectric layer.

The second dielectric layer 24b of the present invention is utilized to induce electron-injection into the floating gate 25 and electron-emission from the floating gate 25, and fulfills the same role as a tunneling oxide layer in a conventional flash EEPROM device. The first dielectric layer 24a is formed to be thicker than the second dielectric layer 24b so that the total capacitance of the floating gate dielectric layer (C2) is educed, and the GCR value increases. Alternatively, if the GCR value is maintained, the capacitance C1 may be reduced, which enables reduction of the size of the unit cell (i.e., width d' of the floating gate 25 - see Fig. 4c). Accordingly, in the present invention, the floating gate 25 may be formed only on the floating gate dielectric layer 24a, 24b (see claim 5).

In contrast, Kurokawa positions and connects the first insulating film 108 on the second region (writing region) 107 and the second insulating (tunnel oxide film) 110 on the first region (writing control region) 106 in a series relationship between the source 103 and the drain 104 so as to reduce the dispersion width of a threshold voltage after repeated writing and erasing, which is the object of Kurokawa.

Also, in the writing mode of the semiconductor device disclosed in Kurokawa, the device is turned by a voltage that is higher than the threshold voltage of EEPROM with the first insulating film 108 or threshold voltage of EEPROM with the second insulating film 110, whichever is higher. In contrast, in the present invention, the insulating film position and connection between the source and the drain is in parallel. Accordingly, the parallel position is advantageous over the serial connection in view of the cell size reduction.

Further, if, in Kurokawa, the connection of the first insulating film 108 and the second insulating film 110 is modified in parallel between the source 103 and the drain 104, as is done in the present invention, the object of Kurokawa, reduction of the dispersion width of a threshold

voltage reduction of the dispersion width of a threshold voltage after repeated writing and erasing, cannot be accomplished.

In addition, in the present invention, the floating gate may be formed only between the field oxide layers, and is not overlapped with the field oxide layers (see amended claim 10 and Fig. 4c of the present invention). In contrast, the floating gate of Kurokawa is overlapped with the field oxide layers (see Fig. 1B of Kurokawa).

Thus, is respectfully submitted that amended independent claims 1, 6 and 11 are not anticipated under 35 U.S.C. §102(e) by Kurokawa et al. (USPN 6,621,130). Since claims 2-3, 7-10 and 12-15 depend from amended claims 1, 6 and 11, respectively, claims 2-3, 7-10 and 12-15 are submitted not to be anticipated under 35 U.S.C. §102(e) by Kurokawa et al. (USPN 6,621,130) for at least the reasons that amended claims 1, 6 and 11 are submitted not to be anticipated under 35 U.S.C. §102(e) by Kurokawa et al. (USPN 6,621,130).

REJECTION UNDER 35 U.S.C. §103:

In the Office Action, at pages 5-6, claims 5-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kurokawa et al. (USPN 6,621,130; hereafter, Kurokawa) in view of Lee (USPN 6,815,283; hereafter, Lee). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

As noted above, amended claim 1 is different from the invention of Kurokawa. In accordance with the arguments cited above, amended claim 1 is submitted to be patentable under 35 U.S.C. §103(a) over Kurokawa et al. (USPN 6,621,130). Since claims 5 and 6 depend from amended claim 1, claims 5 and 6 are submitted to be patentable under 35 U.S.C. §103(a) over Kurokawa et al. (USPN 6,621,130) for at least the reasons that amended claim 1 is submitted to be patentable under 35 U.S.C. §103(a) over Kurokawa et al. (USPN 6,621,130).

The Examiner admits that Kurokawa does not disclose that the thickness of the first dielectric layer is substantially equal to that of a dielectric layer of a peripheral device formed in a flash EEPROM device to control the flash EEPROM device, as is recited in the present claimed invention. Although Lee discloses that the thickness of the first dielectric layer is substantially equal to that of a dielectric layer of a peripheral device formed in a flash EEPROM device to control the flash EEPROM device, Lee recites that the dielectric layer 14 and the insulating film 17 are sequentially stacked (see col. 4, lines 41-44). That is, Lee recites a connectional and positional arrangement of the dielectric layer 14 and the insulating film 17 in series between a source and a drain formed on the substrate, while amended claim 1 recites that the a first dielectric layer and a second dielectric layer are connected and positioned in parallel between a source and a drain formed on the substrate.

Thus, in accordance with the arguments above for Kurokawa, which recite a

connectional and positional arrangement of the first insulating film and the second insulating film in series between a source and a drain formed on the substrate, it is respectfully submitted that amended claim 1 is patentable under 35 U.S.C. §103(a) over Lee (USPN 6,815,283). Since claims 5 and 6 depend from amended claim 1, claims 5 and 6 are submitted to be patentable under 35 U.S.C. §103(a) over Lee (USPN 6,815,283) for at least the reasons that amended claim 1 is submitted to be patentable under 35 U.S.C. §103(a) over Lee (USPN 6,815,283).

Hence, claims 5 and 6 are submitted to be patentable over Kurokawa et al. (USPN 6,621,130) and/or Lee (USPN 6,815,283), alone or in combination.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: April 6, 2005

By: Darleen J. Stockley
Darleen J. Stockley
Registration No. 34,257

1201 New York Avenue, N.W.
Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501